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PATENT
Case No. 10519/30

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Vivek Subramanian et al.

Serial No.: Not yet assigned

Filed: Herewith

For: VERTICALLY STACKED FIELD PROGRAMMABLE NONVOLATILE MEMORY AND METHOD OF FABRICATION

Group Art Unit:

Examiner:

Commissioner for Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Dear Sir:

Prior to commencing the examination of the above-referenced application, please enter the following amendment.

IN THE CLAIMS:

Please cancel claims 1-94.

Please add the following new claims:

1. (New) A process for fabricating a state change element in a 3-D semiconductor memory device comprising the steps of:
forming a semiconductor layer; and
oxidizing at least a portion of the semiconductor layer in a plasma to form an oxide antifuse layer overlying the semiconductor layer.

2. (New) The process of claim 1, wherein the step of oxidizing at least a portion of the semiconductor layer comprises oxidizing at a temperature of no more than about 400°C.

3. (New) The process of claim 1, wherein the step of oxidizing at least a portion of the semiconductor layer comprises a self-limiting oxidation process having an oxidation rate, and wherein the oxidation rate gradually decreases during the oxidation process.

4. (New) The process of claim 1, wherein the step of forming a semiconductor layer comprises forming a layer of polycrystalline silicon doped with a conductivity determining dopant.

5. (New) The process of claim 1, wherein the step of forming a semiconductor layer comprises forming a layer of amorphous silicon.

6. (New) The process of claim 1, wherein the step of forming a semiconductor layer comprises forming a layer of recrystallized silicon.

7. (New) A process for fabricating a memory cell comprising:
forming a steering element; and
forming a state change element adjacent to the steering element,
wherein the state change element includes a dielectric rupture layer, and
wherein the dielectric rupture layer is formed by a plasma oxidation process.

8. (New) The process of claim 7, wherein the plasma oxidation process forms an oxide layer on a semiconductor material within the state change element.

9. (New) The process of claim 7, wherein the step of forming a steering element comprises forming a steering element containing metal elements, and wherein the plasma oxidation process is carried out at a temperature below that at which the metal elements can interdiffuse in the steering element.

10. (New) The process of claim 9, wherein the plasma oxidation process comprises a process carried out at no more than about 400°C.

11. (New) The process of claim 9, wherein the step of forming a steering element containing metal elements comprises forming a refractory metal.

12. (New) The process of claim 9, wherein the step of forming a steering element containing metal elements comprises forming a refractory metal silicide.

13. (New) A process for fabricating a cell in a 3-D semiconductor memory device comprising:
forming a first conductor layer;
forming a first semiconductor layer overlying the conductor layer;
oxidizing at least a portion of the first semiconductor layer in a plasma to form an oxide layer thereon;
forming a second semiconductor layer overlying the oxide layer;
forming a second conductor layer overlying the second semiconductor layer; and
sequentially etching the second semiconductor layer, the oxide layer, the first semiconductor layer and the first conductor layer to form a pillar of the 3-D semiconductor memory device.

14. (New) The process of claim 13, wherein the step of oxidizing at least a portion of the first semiconductor layer comprises plasma oxidation at a temperature of no more than about 400°C.

15. (New) The process of claim 13, wherein the step of forming a first conductor layer comprises forming a conductor layer including metal elements, and wherein the step of oxidizing at least a portion of the first semiconductor layer comprises a plasma oxidation process carried out at a temperature below that at which the metal elements can interdiffuse in the conductor layer.

16. (New) The process of claim 15, wherein the step of forming a conductor layer containing metal elements comprises forming a refractory metal.

17. (New) The process of claim 15, wherein the step of forming a steering element containing metal elements comprises forming a refractory metal silicide.

18. (New) The process of claim 13, wherein the step of sequential etching comprises forming edge regions on the pillar, and wherein the process further comprises oxidizing the edge region using a plasma oxidation process.

19. (New) The process of claim 13, wherein the step of forming a first semiconductor layer comprises forming a layer of polycrystalline silicon doped with a conductivity determining dopant.

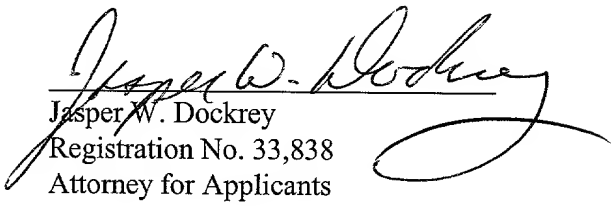
20. (New) The process of claim 13, wherein the step of forming a first semiconductor layer comprises forming a layer of amorphous silicon.

21. (New) The process of claim 13, wherein the step of forming a first semiconductor layer comprises forming a layer of recrystallized silicon.

REMARKS

The Applicants respectfully request entry of this amendment prior to commencing examination of their application.

Respectfully submitted,



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APPENDIX A

IN THE CLAIMS:

1. (New) – 21. (New)